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Description

MULTI-RUN SELECTIVE PATTERN AND ETCH WAFER PROCESS

BACKGROUND OF INVENTION

[0001] Field of Invention

[0002] This invention relates generally to semiconductor wafer manufacturing, and, more particularly, to a method for wafer processing where pre-selected areas of the wafer are treated independently from non-selected areas in a multi-run iterative process.

[0003] The manufacture of semiconductor wafers requires a number of process steps to create a packaged semiconductor device from raw semiconductor material. Patterning silicon wafers involves two coordinated steps, photolithography and etch. Photolithography prints the desired image into photoresist and etching transfers the initial image into the substrate. Metrology of the lithography and etch process steps are a necessary means for measuring the performance of fabrication processes to ensure that specific quality standards are attained. To accomplish this requires a wafer, a measurement tool and the means to analyze the data. Critical lithography and etch quality parameters for wafer production are overlay values; and the critical dimension of the features.

[0004] Lithography is a selective process and can be tailored to specific regions of the wafer. Conventionally etch, contrary to lithography, is not a selective process but a process that affects the entire surface of the wafer. Therefore, when conventionally processing two chip designs requiring different etch properties on a single wafer, obtaining the optimum etch process variables for one-chip design results in the other chip design being etched at less than optimum conditions.

[0005] Conventionally, in order to provide optimum process steps for producing semiconductor wafers, prior art systems often required patterned test wafers to be processed and then cross-sectioned to determine how the processing steps are currently being performed. Conventional wafer production incorporate etch process steps which affect an entire wafer surface, without selectivity to predetermined regions, and result in a high number of scrapped wafers during optimization of the process.

[0006] Additionally, conventional lithography and etch process steps utilized to process Si wafers have a number of limitations. Common limitations encountered during the optimization of wafer manufacturing involve etch regionality effects; line tailoring; and multipart number wafers, where a high number of scrapped wafers results in an increased consumption of wafer material and increased process cost.

[0007] Etch regionality effects is a phenomena whereby the features of the device etch more rapidly in one region of the wafer than the rest of the wafer resulting in a non-uniform etch distribution. For example, when

the wafer etches most rapidly in the center of the wafer, either un-etched features on the outside of the wafer or over-etched features in the center of the wafer can result during etch process steps.

[0008] Line tailoring is where the gates of the device are tailored so that the critical dimension, the channel length, provides the optimum device speed. Tailoring the channel length of the device is achieved by photolithographic striping of the wafer using different image sizes. Each etch experiment conducted in order to optimize etch variables requires the use of a new wafer, since conventional etch process steps effect the entire surface of the wafer. Therefore, conventional line tailoring results in an increased consumption of wafer raw materials due to etch process steps.

[0009] Multi-part number wafers are where multiple designs are produced on a single wafer. Multi-part number wafers are being processed but currently there is no way to compensate for the different etch requirements for different wafer designs, which is a limitation to designers.

[0010] Due to the above limitations a large number of wafers are routinely scrapped during etch experimentation and optimization. Etch experiments require many wafers in order to account for the number of variables in the etch process. The increased consumption of raw materials during process optimization is further amplified by increasing wafer size.

[0011] What is needed is a multi-run wafer production method having a regional selective etch treatment that overcomes the limitations of the current process steps.

SUMMARY OF INVENTION

[0012] The present invention provides a method of multi-run wafer production where predetermined regions of a semiconductor wafer are selectively etched throughout wafer production. One aspect of the present invention in broad terms is a method for processing a semiconductor wafer comprising the steps of:

[0013] a)etching one or more first regions of a wafer according to a first set of etch variables, where a remaining portion of said wafer is prevented from being etched; and

[0014] b)etching one or more other regions of said remaining portion of said wafer according to another set of etch variables, wherein one or more previously etched first regions and any remaining portion of said wafer is prevented from being etched.

[0015] Another aspect of the present invention is a method for processing a semiconductor wafer comprising the steps of:

[0016] a)doping at least one first region of a wafer with a first set of doping variables, where a remaining portion of said wafer is prevented from being doped; and

[0017] b)doping one or more other regions of said remaining portion of said wafer according to another set of doping variables, wherein one or

more previously doped first regions and any remaining portion of said wafer is prevented from being doped.

[0018] Step b) of the above methods may be performed N times, where N is a whole number equal to or greater than one.

[0019] Specifically, a wafer is provided and patterned using photolithographic process steps. Photolithography is the process, which sets the surface dimensions on the various parts of the wafer. Patterning is a basic operation that removes specific regions of the top layers on the wafer surface. The processed regions are pre-selected areas that may be determined by customer specifications. The pre-selected areas can be defined by performance results, as defined by the manufacturer or customer, or by modeling.

[0020] In the present invention a layer of photoresist is patterned to protected pre-selected areas of the wafer, where the exposed areas of the wafer not protected by the photoresist are etched according to customer specifications. Conventionally, the etch or implant processes affect the entire surface of the device. The present invention, by applying a patterned photoresist to pre-selected areas of the wafer prior to etch process steps, protects those areas during the first etch process. Once the resists are removed etching of another pre-selected area during a second etch may be performed. This process allows for multiple etch process steps with different etch variables to be applied to one wafer.

[0021]

First, a photo resist layer is provided where the photo resist layer is

selectively exposed resulting in a combination of patterned and unpatterned portions of photoresist on the wafer surface. Patterning comprises transferring an image to a light sensitive layer of photoresist where the image is produced by a recticle having an opaque region. In one aspect of the present invention the light image determines a first region and at least one other region of the wafer. When the wafer is etched only the portions of the wafer exposed to the light image are affected. Ideally, a pattern is provided on the surface where the pattern dimensions are as close to the design requirements as possible. The pattern dimensions are referred to as the image sizes of the circuit.

[0022] Following the photolithography process steps the exposed fields can then be subject to an etch process. Etch chemistries selective to the photoresist remove the portion of the wafer not covered by the photoresist. It is in the etch process step where the image created in the photolithography process step is permanently transferred into the surface layer of the wafer. After etching, the pattern is a permanently transferred into the top layer of the wafer, preferably an oxide layer. The resist layer that has acted as an etch barrier is no longer needed and is removed from the surface. The resist layer can be stripped using a wet chemical process.

[0023]
A second pattern is then applied to the surface of the wafer. The second pattern is positioned to etch the regions of the wafer that were protected by the photoresist during the first etch process steps. Following the application of the second pattern, the wafer is etched and

the resists is removed. This process can be repeated numerous times until the desired conditions are attained. Using the above described process the number of etch experiments may be reduced in order to produce optimum processing conditions, therefore reducing raw material consumption.

[0024] Alternatively, predetermined regions of a semiconductor wafer may be selectively doped by using the above-described method and substituting implant process steps for etch process steps. Another aspect of the present invention is to incorporate both implant process steps and etch process steps.

BRIEF DESCRIPTION OF DRAWINGS

[0025] FIG.1 is a pictorial representation (through cross sectional view) showing the initial semiconductor wafer structure.

[0026] FIG.2 illustrates a flow diagram of a multi-run selective pattern and etch wafer process.

[0027] FIG.3 is a pictorial representation (top view) of a waferhaving both patterned regions and exposed portions.

[0028] FIG.4 is a pictorial representation (top view) of a waferexhibiting regionality effects.

[0029] FIG.5 is a pictorial representation (top view) of a waferexhibiting line-striping effects.

[0030]

FIG.6 is a pictorial representation (top view) of a waferwhere the

photolithography dosage and etch bias is increased across the wafer surface.

[0031] FIG.7 is a pictorial representation (top view) of a waferexhibiting multi-part number effects.

[0032] FIG.8 illustrates a flow diagram of a multi-part number multi-run selective pattern and etch wafer process.

DETAILED DESCRIPTION

[0033] The present invention, which provides a multi-run wafer production method having a selective region etch treatment or implant, will now be discussed in greater detail by referring to the drawings that accompany the present application. It is noted that in the accompanying drawings like reference numerals are used for describing like and corresponding elements.

[0034]

Referring to FIG. 1, a wafer *1* is provided preferably including a layered stackatop a substrate *6*. The layered stack comprises of at least one material layer, preferably being an oxide layer *3* such as SiO_2, atop a thin layer of nitride 4, such as Si_3N_4 or other like materials including but not limited to SiN. The material layer may comprise alumina, polysilicon (poly-Si), silicon, copper, TiN, TaN, oxide, nitride, polyimide or combinations threeSof, preferably being oxide material. ubstrate materials include but are not limited to: any semiconducting material such as Si, SiGe, GaAs, InAs and other like semiconductors. Additionally, the substrate could further include a conducting layer or

metal layer comprising Cu, or Al positioned at the top surface of the substrate. The thin nitride layer 4 prevents electro-migration and acts as an etch stop layer. TAlthough te nitride layer 4 aacts asan etch stop in order to protect the underlying substrate from etch and corrosion during etch process steps selective to removing oxides., it is not a required layer in all of the various layered stacks embodied in the present invention

[0035] Referring to FIG. 2, an initial photolithography process is performed atop wafer 1, as depicted in block 10. In general, the initial photolithography process steps define the pre-selected protected regions of the wafer that are not etched and which regions of the wafer are to be exposed and therefore etched during the first etch process run. Alternatively, the initial photolithography process steps define the pre-selected protected regions of the wafer that are not to be doped or implanted and which regions of the wafer are to be exposed and therefore doped using implant process steps. The regions of the wafer are defined by the opaque image pattern of the reticle and through the use of blinders. The photolithography steps are now described in more detail.

[0036]

A thin layer of photoresist material is applied atop the wafer via spin coating or similar processes. The photoresist material comprises of dielectrics including carbon, oxygen, and various inorganic materials. Following application of the photoresist layer, the photoresist is soft-baked, where the solvents of the photoresist layer are evaporated via

heating.

[0037] The layer of photoresist is then patterned using a photolithography process as depicted in block 10 of FIG. 2. A patterned photoresist is formed utilizing conventional photolithography and etch process steps. Specifically, a pattern is formed using a reticle or photomask and transferred into the surface of the wafer. First, the pattern on the reticle or photomask is transferred onto a layer of photoresist on the surface to be etched, or alternatively implanted. Light is passed through the opaque pattern of the reticle, which in turn produces a patterned image on the layer of photoresist. The photoresist layer is a light or radiation sensitive material and exposure to light causes changes in the photoresist structure. For example, exposure to light may change the exposed portions of the photoresist from a soluble condition to an insoluble one. In addition to the patterns produced by the reticle, regions of the wafer may be selectively patterned by adjusting the step plan of the photolithography tool to avoid exposing specified areas. The step plan adjustment is a determination of which fields to expose. Normally the lithography tool prints every field in a tight matrix or checkerboard pattern to maximize the number of chips on a wafer. An aspect of the present invention is to manipulate the step plan in order to selectively expose each desired field. The opaque reticle pattern and reticle blinders may be used together or separately. FIG. 3 depicts an example of a wafer 1 having both patterned regions 5 and exposed portions 3.

[0038] Following exposure the pattern is developed utilizing conventional developer, such as a chemical solvent. The developer leaves a hole in the resist layer that corresponds to the opaque pattern of the reticle. An alternative resist strategy, commonly referred to as a negative resist, leaves a pattern in the resist opposite to that on the mask. Development of the pattern is conducted using conventional development techniques including, but not limited to: continuous spray development and puddle development.

[0039] Referring back to FIG. 2, once the initial photolithography process is completed, a metrology-data acquisition procedure is performed on the processed semiconductor wafer using conventional measurement/analysis tools, as depicted in block 15. Metrology is the science of measurement to determine dimensions, quality, and capacity. Metrology during fabrication employs measurement equipment and sensors to collect and analyze data about wafer parameters and defects.

[0040] Alignment or correct placement of the circuit pattern is critical issue in the photolithographic process step. The entire circuit pattern must be correctly placed on the wafer surface and the individual parts of the circuit must be relative to each other. During photolithography in addition to dimension control and pattern alignment, defect control is also critical.

[0041] Some of the metrology tools utilized include, but are not limited to: SEM, overlay, and defect inspections. The metrology data is then

analyzed and if a pattern is out of specification or exceeds dimension tolerance limits a rework step as known in the art, may be conducted.

[0042] Once the patterning of the photoresist is completed, the regions of the oxide layer of the wafer covered by the photoresist are protected while the exposed regions are removed using a selective etching process that removes the unprotected regions. The sections covered by the resist are protected because the chemistry of the resist is such that the resist does not dissolve under etch process steps.

[0043] AThe material layer is then etched. When etching a material layer comprising the preferred oxide material, a oxide etch process is performed on the wafer with an integrated resist strip, as depicted in block 20 of FIG. 2. This etch process will include an ARC (anti-reflection coating) breakthrough step, a dielectric etch step, and a resist strip step. The process chemistries may include, but are not limited to: $CF4_4$ $O2_2$ $CHF3_3$ $CH3_3$, $C4_48_8$ CO, or Ar. Etching of the substrate is performed using a conventional timed etch process step that is highly selective in removing oxide as opposed to nitrides and forms a trench structure into the wafer surface. Conventional dry etching processes that may be employed include, but are not limited to: Reactive Ion Etch (RIE), ion-beam etching, plasmaaetching, etc. Etch compositions that may be utilized for etching the oxide layer include HF, $CF4_4$ $O2_2$ $CHF3_3$ $CH3_3$, $C4_{48}$, CO, or AArgon. Alternatively, material layers comprising alumina, polysilicon (poly-Si), silicon, copper, TiN, TaN, nitride, and polyimide may be etched

[0044] Alternatively, instead of etching the exposed regions in block *20,* the exposed surfaces may be doped using convention implant process steps. Dopants are selected depending on the performance required of the device. For example, P-type device dopants for Si are Group III-A elements, such as boron, while the N-type device dopants are Group V elements, such as phosphorus. Doping variables include dopant species, dopant concentration, and implant energy.

[0045] An integrated resist strip step may be incorporated with the omaterial layeretch or implant process step. A number of different chemicals mayb e used for stripping and are dependent on the wafer surface, production considerations, the polarity of the resist, and the condition of the resist. Preferably, solutions of sulfuric acid and an oxidant, such as hydrogen peroxide or ammonium persulfate, or plasmas containing $CF4_4$ $N2_22_2$ and O_2 are used for stripping the dielectric photoresist.

[0046]

Once the omaterial layeretch process is finished, a standard etch metrology is performed as depicted in block 25 of FIG. 2. A determination is made whether the pre-selected areas of the wafer are within the predetermined engineering specifications. The properties of the pre-selected areas, which are based on the omaterial layeretch process metrology data of the semiconductor wafer being processed, are compared to a set of predetermined optimum properties. The set of predetermined minimum properties and predetermined maximum properties are generally customized for the particular type of semiconductor devices being manufactured. There is an etch

component to the final measurements, called an etch bias. Etch bias is the difference between the critical dimension of the patterned photoresist layer and the etched region of the device. Etch bias influences the etched image size.

[0047] Etch metrology may be conducted by manual microscope inspection and automatic inspection tools similar to the inspection tools used in aforementioned photolithography inspection. The etch metrology process step *25* is very similar to initial metrology, except that there is no photoresist and defective wafers cannot be reworked. One measurement that occurs during etch metrology is the automated measurement to verify critical dimension on a particular mask level. Generally, the quality of the etch process is verified by inspection for etch problems such as over-etching, under-etching, and undercutting.

[0048] Alternatively, the above described etch metrology step may be configured for evaluating doped regions formed during implant process steps. Defectively implanted wafers, similar to defectively etched wafers, may not be reworked.

[0049] Following etch metrology *25* an SP (Sulfuric Peroxide) clean step *30* is performed where any remaining polymer residue is removed from the wafer by a chemical cleaner. The cleaner may comprise of a 30% HF solution or sulfuric acid composition however other compositions may be used.

[0050]

The first photolithography and etch process or implant run concludes

with a run analysis process step *35* that determines whether another photolithography and etch process or implant run is to be performed. The etch variables of a second etch process may be different from the first etch process. Etch variables that may be changed in the subsequent iterations may include, but are not limited to: etch time, etch chemistry, etch concentration, tool chuck temperature, tool wall temperature, plasma power, or gas ratios or flows. The decision to run a second photolithography and etch process or implant run may be part of the original process flow. The etch variables of a second etch process may be different from the first etch process. Etch variables that may be changed in the subsequent iterations may include, but are not limited to: etch time, etch chemistry, etch concentration, tool chuck temperature, tool wall temperature, plasma power, or gas ratios or flows. TThe doping variables of a second implant process may be different from the first implant process. Doping variables include dopant species, dopant concentration, and implant energy. The decision to run a second photolithography and etch process or implant run may be part of the original process flow.

[0051]

If there are more regions/chips on the wafers surface that need to be processed or if a determination is made that the properties of the selected areas are insufficient, the above-described process steps may be repeated for each region/chip. More specifically, if a second run is conducted the following process steps are repeated on the same wafer in the order as presented: photolithographic process steps *10*, initial

metrology *15*, oxide etch *20*, etch metrology *25*, SP clean *30*, and process analysis *35*.Alternatively, implant process steps may be substituted for oxide etch *20* process steps. Iteration of these process steps may be repeated numerous times for different pre-selected areas until the desired conditions are attained. With each iteration the etch process variables or implant variables may be changed.

[0052] Once a determination is made at step *35*, that the selected areas are sufficiently processed during patterning and oxide etch, a standard nitride etch process step is conducted, as illustrated in block *40* of FIG. 2. The standard nitride etch *40* is a blanket process where the etch process is selective to removing the nitride layer without attacking the underlying substrate. Conventional dry etching processes that may be employed include, but are not limited to: Reactive Ion Etch (RIE) and plasma etching. When the nitride layer comprises silicon nitride, etch concentrations may include, but are not limited to: CF4,$_4$O2,$_2$N2,$_2$or Argon may be utilized as an etch composition. Following nitride etch step 40, an etch metrology process step 45 is conducted that is similar to the etch metrology process step 25. At this point the wafer has been etched sufficiently to allow communication between the wafer and interconnect wiring atop the wafer during metallization formed during later conventional processing steps 50.

[0053]
In one embodiment of the present invention the lithography and etch process steps are tailored to overcome the limitations of etch regionality effects. Etch regionality effects are where the features of the pattern

etch more rapidly in one region of the wafer than in the rest of the wafer. Etch regionality effects result in insufficiently etched areas where the etch process is slow or over-etched regions where the etch process is most rapid. In one example, the center of the wafer etches most rapidly resulting in un-etched features on the outside of the wafer or over-etched features in the center of the wafer.

[0054] According to the present invention, etch regionality effects are overcome by running multiple photolithography and etch process runs on a single wafer. Referring to FIG. 4, depicting a wafer surface having etch regions A and B, if one area of the region A etches at a faster rate than the rest of the wafer, the fast etching region A is selectively exposed while the remaining portion B of the wafer is protected by blanket resist. Following photolithography, the features of the exposed portion A are etched while the regions covered by the resist B are protected. After the etch is complete the resist is removed and the surface of the wafer is cleaned. Thereafter, the wafer is treated to a second lithography process step where the fast etching region A of the wafer is protected by a second resist while the slower etching portion B of the wafer, that was protected during the first etch process, is exposed. A second etch process is then conducted where the features of exposed slower etching region B of the wafer are etched while the features of the faster etching region A are protected by the overlying second resist. The second pattern is then stripped and the wafer is cleaned.

[0055] Using this multi-run method the etch variables for optimum etching can be tailored to both fast A and slow B regions of the wafer, therefore overcoming etch regionality effects. Therefore, using the present invention at least one pre-selected region of the wafer can be etched using one etch variable while a secondary region of the wafer can be etched using a second etch variable. Alternatively, the same operating scenario utilized to overcome etch regionality can be employed with implant process steps in order to more accurately control dopant concentration throughout the wafer during implant process steps.

[0056] According to a further aspect of the invention, the photolithography and etch process steps may be tailored to process one particular field or area having a higher pattern density or different line size than the rest of the pattern. The area of the wafer having a higher pattern density will react differently to etch and lithography process steps than the rest of a wafer. To overcome these differences, photolithography process steps could be implemented to pattern and expose the entire field without exposing the particular portion of the wafer having a higher etch density or different line width. Then, a second series of photolithography and etch process steps may be performed where the region of higher etch density or different line width is exposed and etched while the remaining portion of the wafer is protected by photoresist. Using this method both the region of higher pattern density and the remaining portion of lower pattern density can be optimized.

[0057]

In another embodiment of the present invention, the photolithography

and etch process steps are configured to overcome the limitations of line tailoring. Line tailoring is the dimensioning of the gates of a device, such as a FET, so that a critical dimension, the channel length, is tailored for the optimum device speed. Conventionally, tailoring the channel length of the device is achieved by patterning the wafer to form photoresist striping and utilizing multiple photolithography process steps of different image sizes. Each stripe of photoresist formed on the wafer is of a different width, preferably increasingly smaller. For example, a first photoresist strip of a first width is formed atop a wafer during a first photolithographic pass followed by the formation of a secondary photoresist strip of photoresist having a second width during a second photolithography pass. FIG. 5 depicts line striping across the surface of a wafer where line stripes are depicted as shaded vertical columns and vertical columns having a blank fill, where each line stripe has a line width W.

[0058] Etch chemistry is also an important component of line tailoring. Conventional etch processes affect the entire surface of the wafer without selectivity of specific regions. Using conventional processing, each time the etch variables are changed a new wafer must be etched in order to optimize the etch process. Therefore, conventional etch process steps limit line tailoring experimentation of a wafer to one pass through the etch process step for each etch composition.

[0059] One aspect of the present invention allows for both photolithographic line tailoring and etch line tailoring where a wafer may be optimized

using a reduced number of wafers by subjecting a single wafer to multiple photolithographic process steps and multiple etch process steps each selective to a specific region of the wafer. In the present invention line tailoring can be accomplished solely using photolithography, solely using multiple etch process steps, and a combination of both etch process steps and photolithography, as described with respect to FIG. 2, steps 10 and 20.

[0060] In order to optimize line tailoring while overcoming the disadvantages associated with conventional line tailoring, the present invention includes photoresist striping of the wafers using conventional lithography. Next, an etch matrix is produced which is comprised of multiple process passes that have different etch process conditions which are designed to change the effective etch bias (e.g. the amount of change in critical dimension from the post-lithography measurement to the post-etch measurement). This allows for etch process steps to be selectively applied to specific regions of the wafer. By providing a method to expose different regions of a single wafer to multiple etch process steps, incorporating different etch variables and etch chemistries, optimization is achieved more quickly, while reducing the number of scrapped wafers.

[0061]

FIG. 5 depicts an example of a line tailoring pattern formed using a multi-run wafer process, comprising two photolithography process steps and two etch process steps, where the regions of the wafer treated during the photolithography process steps (of FIG. 2) are depicted

using reference letters A' and B' and the regions of the wafer treated during etch process steps are depicted by reference letters C and D. In lithography, different critical dimension sizes can be created by different focus conditions or other such variables including, but not limited to: focus, resist type, or tooltype. Etch may vary conditions including etch times, temperatures, voltages, or chemistries to obtain the optimal process. The regions treated during the etch process steps C, D depict an etch matrix. The etch matrix is defined during photolithography process steps, where the regions are selectively etched using recticle patterning or applying photoresist atop photolithographic areas using patterning and further defining exposed regions with reticle blinders.

[0062]

Another aspect of the inventive method for line tailoring allows for a series of etch line striping steps where following photo resist line striping formed using photolithography, a matrix of increasing etch bias is utilized to further decrease the photoresist line width W and further decrease resultant device gate size. The concentration of photolithography dose and etch bias is pictorially represented in FIG. 6, where the arrows indicate increasing photolithography exposure 60 or etch increasing bias 65 respectively. Assuming positive resist, gate size decreases with increasing dose and positive etch bias. Therefore, varying the etch bias and exposure will determine a process window and optimum value for both processes. Typically, line width W decreases with increasing exposure across the wafer 1 in FIG. 6. Additionally, implant process steps may be utilized to increase the

dopant concentration. By increasing the concentration of dopants the device switching speed is increased. Using the above described process the exposed portion of the wafer is doped by substituting conventional implant process steps for etch process steps.

[0063] A further embodiment of the present invention provides photolithography and etch process steps configured to overcome the limitations of conventional processing of multipart numbered wafers. Referring to FIG. 7, multi-part number wafers are conventionally produced using one photoresist mask to pattern two or three different regions for producing different designs within the wafer, such as design 1 on region A" and design 2 on region B". Pattern densities utilized on wafer designs may vary up to 300% due to etch loading, nested/iso offsets and the like. Conventional wafer production process methods can not compensate for such differences; rather, conventional process steps optimize the conditions for one design, such as design 1 on region A", while sacrificing conditions for the other, design 2 on region B". Conventionally, both region A" and region B" get the same processing since both region A" and B" are treated using the same photolithography step and the same etch step. Therefore using the conventional process flow, one can not tailor the etch process steps to the requirements of the regions A" and B" separately.

[0064] Using the inventive method, section A" may be processed through photolithography, etch and optional rework process steps and then region B" may be processed using a second photolithography and etch

process. During the processing of region B" both the photolithography process as well as the etch process steps may be varied from the etch and photolithography process steps utilized to process region A". The photolithography process steps may be varied by changing the numerical aperture, the photomask image, resist type, exposure, focus, tool type. The etch process steps may be modified by varying the geography of flow, temperature, and etch chemistries. Although the above example illustrates only two chip designs, multiple chip designs are also contemplated and included therein. Alternatively the above described resist pattern can be utilized during implant process steps so that a number of different dopant species can be introduced to specific pre-selected regions of a single wafer.

[0065] In addition to photo masking sections A" and B" reticle blinders may also be utilized to expose specific regions of the wafer without exposing the entire wafer. This process step is depicted in new block 5 of the flow diagram illustrated in FIG. 8, which otherwise is identical to the process depicted in FIG. 2.

[0066] The inventive method for wafer production also allows for etching of pre-selected specific areas of the wafer in order to compensate for a higher or lower occurrence of nested or isolated wire, or greatly varying RX pattern densities without etching the remaining portions of the wafer. As wafer sizes increase and more part numbers are linked, it will become more and more difficult to group parts with similar pattern densities and designs, making this aspect of the present invention an

important option for improving yield and manufacturability.

[0067] By using the above method the problems of etch-regionality, over-etching, and under-etching are overcome and a more uniformly etched wafer is provided. Additionally, the etch process variables may vary during each etch iteration to further optimize the process.

[0068] While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.